NATIONAL UNIVESITY OF SCIENCE AND TECHNOLOGY

DEPARTMENT OF APPLIED PHYSICS

SPH 1202 – ANALOGUE ELECTRONICS

BSc HONOURS PART I: MAY 2006 *DURATION: 3HOURS*

ANSWER **ALL** PARTS OF QUESTION **ONE** IN SECTION **A** AND ANY **THREE** QUESTIONS FROM SECTION **B**. SECTION **A** CARRIES 40 MARKS AND SECTION **B** CARRIES 60 MARKS.

SHOW ALL YOUR WORKING STEPS CLEARLY IN ANY CALCULATION.

SECTION A

1. (a) Write down the diode current equation and state the meaning of each symbol used. The reverse saturation current at room temperature is 0.3μA when a reverse bias is applied to a Germanium diode. Find the value of the current flowing in the diode when 0.15V forward bias is applied at room temperature. [4]

   (b) Explain what is meant by capacitance of a pn junction. Write down the expression for the dynamic transition capacitance. [6]

   (c) A supply with an output resistance of 1.5Ω supplies a full load current of 500mA to a 50Ω load.
   (i) What is the percent voltage regulation?
   (ii) What is the no load output voltage of the regulator? [4]

   (d) Write down the basic differences between the BJT and FET. Give the characteristics of the JFET defining drain resistance and transconductance. [6]

   (e) A load $R_L = 200\Omega$, is to be supplied with 75V at 40mA for a full wave rectifier with an L- section filter consisting of L = 10H and C= 10μF. Find the ripple factor for a given frequency, f = 50Hz. [4]

   (f) A tuned oscillator has a resonant frequency of 5MHz. If the value of the capacitance is increased by 50%, calculate the new resonant frequency. [5]

   (g) Differentiate between intrinsic and extrinsic semiconductors. [3]

(h) Draw the circuit diagram of an inverting integrator and deduce the expression for its output. [6]

(i) What is the difference between a clipping and a clamping circuit? [2]

SECTION B

2. (a) Determine the operation of an npn transistor circuit shown below. Sketch the dc load line and show the Q- point. Assume that R_B = 390kΩ , β= 100; $V_{CE(sat)}$ = 0.2V ; and V_{BE} = 0.7V. [10]

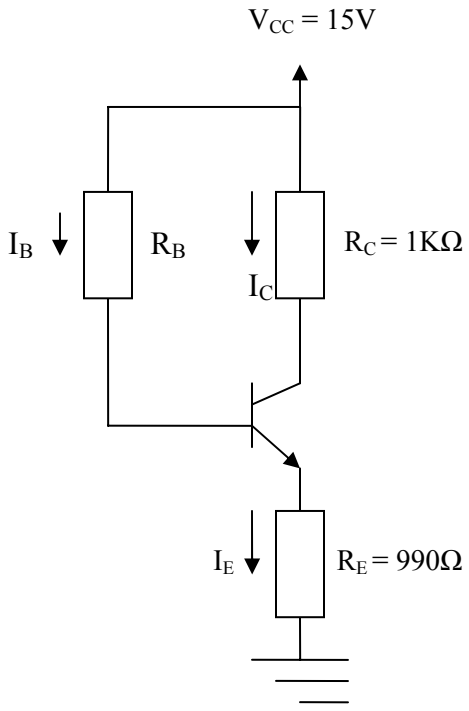

Figure 1.

(b) Explain the operation of a series voltage regulator. [6]

(c) State two amplifier – coupling methods giving one advantage and one disadvantage of each method. [4]

3. (a) A common- remitter amplifier uses a voltage source with internal resistance $R_s = 800\Omega$, and a load resistance $R_L = 1000\Omega$. The h – parameters are $h_{ie} = 1k\Omega$; $h_{re} = 2 \times 10^{-4}$; $h_{fe} = 50$ and $h_{oe} = 25\mu AV^{-1}$. Calculate;

(i) the current gain, A_i ;

(ii) the input resistance, R_i and

(iii) the voltage gain, A_v. [6]

(b) State the meaning of each of the h- parameters used above. [4]

(c) Draw the diagram of a Wien- bridge oscillator and deduce the equation for its output frequency. [10]

4. (a) Draw a diagram of a centre-tapped rectifier and sketch the output voltage in response to a 12V r.m.s ac input. Explain why the output has the form it does in terms of the operation of the centre tap circuit. [8]

(b) Deduce an equation for the ripple factor of a full wave capacitor-filter rectifier, stating all the relevant approximations. [8]

(c) Draw a block diagram of an oscillator and state the conditions necessary for oscillations to take place. [4]

5. (a) Design a common-emitter amplifier that delivers 0.5W power to a 100Ω resistor. Use a transistor that has a maximum current rating of 500mA, collector-to-emitter saturation voltage of 0.5 V, breakdown voltage of 40V, and the common-emitter current gain of 100. [10]

(b) Describe briefly the operation of a JFET. [4]

(c) Draw a biased npn and pnp transistor. Label all the currents and show the direction of flow. How are all the currents of the transistor related? [6]

6. (a) Explain the features of the following filter formats:
(i) butterworth,
(ii) chebyshev,
(iii) Bessel. [9]

(b) Two voltages + 0.6V and -0.4V, are applied to the two input resistors of a summation amplifier. The respective input resistors are 400kΩ and 100kΩ, and the feedback resistor is 200kΩ. Draw the circuit diagram and then determine the output voltage. [7]

(c) A transistor amplifier stage comprises a FET, of parameters $Y_{fs} = 2.2mAV^{-1}$ and $Y_{os} = 20\mu s$, and bias components and coupling capacitors of negligible effect. The total load on the output is 2kΩ. Determine the voltage gain. [4]