NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

SPH 2106 Digital Electronics

SUPPLEMENTARY EXAMINATION

BSC HONOURS PART II : JULY 2003 **DURATION : 3 HOURS**

ANSWER ALL QUESTIONS IN SECTION A AND ANY THREE QUESTIONS FROM SECTION B. SECTION A CARRIES 40 MARKS AND SECTION B CARRIES 60 MARKS.

Planck's Constant	$h = 6.63 \times 10^{-34}$ Js
Boltzmann's Constant	$k = 1.38 \times 10^{-23}$ JK^{-1}
Speed of light	$c = 3.00 \times 10^{8}$ ms^{-1}
Charge on an electron	$e = 1.60 \times 10^{-19}$ C
Mass of an electron	$m_e = 9.10 \times 10^{-31}$ kg
Permittivity of free space	$\varepsilon_o = 8.85 \times 10^{-12}$ Fm^{-1}
Permeability of free space	$\mu_o = 4\pi \times 10^{-7}$ Hm^{-1}

SECTION A

1. (a) Convert the following numbers into binary numbers:

(i) ~~$3BSD_{16}$~~, (ii) 7543_8 (iii) 575.375_{10} and (iv) 175.275_8

[4]

(b) Find the value of the following binary operations:

(i) 110111 ÷1011, (ii) 11101* 1110 (iii) 11110 + 11011 + 11101 and

(iv) 10111- 1011

[4]

(c) Write the following numbers in 8421 and 2421 coding systems:

(i) 1475_{10} and (ii) 555_8

[4]

(d) Use K-map to simplify the following Boolean expressions:

(i) $F(ABC) = \overline{A}B\overline{C} + \overline{A}BC + AB\overline{C} + ABC$

(ii) $X = \overline{A}\left(BC + B\overline{C}\right) + A\left(BC + B\overline{C}\right)$

[8]

(e) State and prove De Morgan's theorem. Use the theorem to minimize following functions:

(i) $(A+B)(\overline{A}+C)(B+C)=(A+B)(\overline{A}+C)$

(ii) $A+BC=(A+C)(A+B)$

[8]

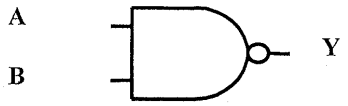
(f) Draw the diagrams for the four input multiplexers and four output demultiplexers. Give one application of each of them.

[6]

(g) Explain the terms: (i) Logic threshold, (ii) Noise Margin and (iii) Propagation Delay.

[4]

(h) How will you realize the following logic using DTL? Give truth table for its operation.



[2]

SECTION B

2. (a) Show that the "NAND" and "NOR" gates are universal gates.

[7]

(b) A gate is required to monitor two lines, to detect the occurrence of "LOW" level voltages on either or both lines, and to generate a "HIGH" level output used to illuminate an indicator lamp. Draw the circuit and explain the operation.

[7]

(c) A certain gate draws a current of 2 mA when its output is "HIGH" and 3.5 mA when its output is "LOW". What is the average power dissipation if V_{CC} is 5V and is operated on 50 % duty cycle?

[6]

3. (a) What is the difference between half-adder and full-adder?

[4]

(b) Determine the method for implementing full-adder.

[8]

(c) Describe the methods of speeding addition.

[8]

4. (a) Draw a diagram for the four stage Johnson Counter. Give the truth table and explain the operation of the counter.

[8]

(b) Draw a ten stage ring counter and show table of its sequence.

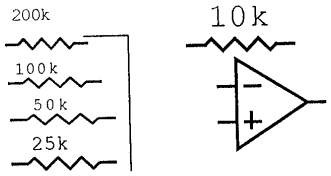
[5]

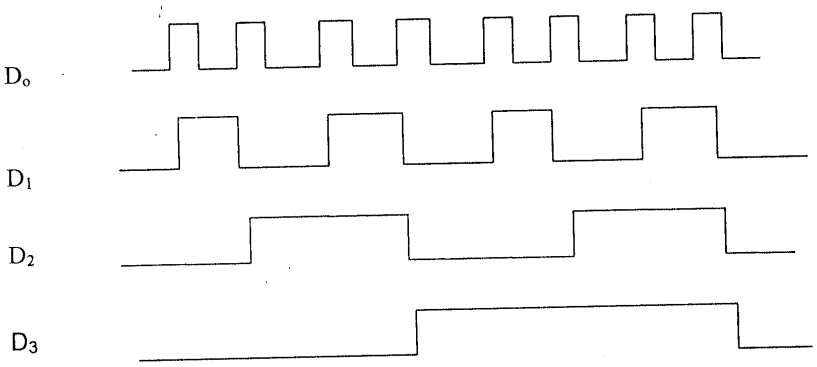
(c) If the ten stage ring counter has the initial stage 1010000000, determine the waveform of the Q outputs. [7]

5. (a) Give the performance characteristics of D/A Converter. [4]

(b) Draw the circuit diagram of a "Four Bit Binary Weighted input D/A converter. Explain its operation. [8]

(c) Determine the output of the D/A converter shown below for the sequence of four bit numbers that are applied to the inputs. D_o is the LSB. [8]





6. (a) Draw a neat diagram of a "Dual Slope A/D converter and explain its operation. [10]

(b) Explain the terms:

(i) Resolution, (ii) Sampling Rate and (iii) UART [6]

(c) Determine the resolution for each of the following D /A converters.

(i) Four bit, (ii) six bit and (iii) 18 bit.

[4]

END OF PAPER