NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

APPLIED PHYSICS DEPARTMENT

SPH 2106 - DIGITAL ELECTRONICS

BSc HONOURS PART II: MAY 2005 *DURATION: 3 HOURS*

ANSWER **ALL** PARTS OF QUESTION **ONE** IN SECTION A AND ANY **THREE** QUESTIONS FROM SECTION B. SECTION A CARRIES 40 MARKS AND SECTION B CARRIES 60 MARKS.

SECTION A

1. (a) What is encoding? [4]

   (b) Distinguish between the following:
   - (i) Binary-Coded-Hexadecimal (BCU) [4]
   - (ii) Binary-Coded-Decimal (BCD) [4]
   - (iii) Binary-Coded-Octal (BCO) [4]

   (c) Convert the following number to BCD
   - (i) 63.7608_{10} [2]
   - (ii) 1769_{10} [2]
   - (iii) 563_{10} [2]

   (d) State two advantages of straight binary system over BCD in the computer? [4]

   (e) Convert
   - (i) 10110011.110011_2 to hexadecimal [3]
   - (ii) 0.0000011101_2 to hexadecimal [3]
   - (iii) $DC6.AF4_{16}$ to binary [2]

   (f) Distinguish between
   - (i) Most Significant Bit (MSB) [2]
   - (ii) Least Significant Bit (LSB) and [2]
   - (iii) Parity or check Bit [2]

SECTION B

2. (a) Define each of the following:
   - (i) commutative property [2]
   - (ii) associative property [2]
   - (iii) distributive property [2]
   - (iv) De Morgan's theorem. [2]

(b) Construct a truth table for the Boolean expression.

(i) $F = \overline{A\ \overline{B} + \overline{C}}$ [2]

(ii) $F = \overline{(A+B+C)DE}$ [2]

(c) Draw a minimum configuration logic diagram to represent the statement:

(i) $F = ABC + \overline{B} + C$ [3]

(ii) $F = \overline{\overline{A}\ B + A\ \overline{\overline{C}} + \overline{B}\ \overline{C}}$ [3]

(d) Prove that

(i) $(A+B)\overline{AB} = A\ \overline{B} + \overline{A}\ B$ [2]

3. (a) Expand the following acronyms for different families of logic gates

(i) RTL [1]
(ii) DTL [1]
(iii) TTL [1]

(b) Explain with the aid of diagrams the three different switching modes of bipolar intergrated circuit (Ic) gates. [12]

(c) Define the terms

(a) logical 1 [1]
(b) logical 0 [1]
(c) fan out [1]
(d) noise margin [1]
(e) propagation delay [1]

4. Commercial Bank X requires three "black box" units. The performance of the first unit is summarised by truth table 1 below.

Truth table 1

INPUT			**OUTPUT**
SW1	*SW2*	*SW3*	*ALARM*
OFF	OFF	OFF	OFF
OFF	OFF	ON	OFF
OFF	ON	OFF	OFF
OFF	ON	ON	ON
ON	OFF	OFF	OFF
ON	OFF	ON	OFF
ON	ON	OFF	ON
ON	ON	ON	ON

The operation of the second "black box" unit is described by the Boolean expression:

$$OUTPUT = \overline{A}\ \overline{B}\ \overline{C} + A\ \overline{B}\ \overline{C} + \overline{A}\ \overline{B}\ C + \overline{A}\ \overline{B}\ C + A\ \overline{B}\ C$$

The Boolean expression for the third "black box" unit is:

$$OUTPUT = AB\overline{C}D + A\overline{B}\overline{C}D + A\overline{B}CD + ABCD$$
$$+$$
$$A\overline{B}CD + ABC\overline{D} + A\overline{B}C\overline{D} + \overline{A}\overline{B}CD$$
$$+$$
$$\overline{A}BCD + ABCD + A\overline{B}CD + \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}C\overline{D}$$

(a) Use the Karnaugh map (K - map) technique to simplify the respective Boolean expressions. [10]

(b) Draw a minimum - configuration circuit for each simplified expression. [10]

5 (a) Draw a logic diagram for an RS flip - flop using:

(i) NOR gates [2]
(ii) NAND gates [2]

(b) Explain in brief the

(i) Advantages of a gated RS flip-flop one over a RS flip-flop [2]
(ii) Advantage of a JK over a master-slave RST flip flop [2]
(iii) Race condition and how it is solved [4]
(iv) Disadvantages of the master-slave RST flip-flop [2]

(c) Define each of the following:
(i) astable
(ii) bistable
(iii) monostable [6]

6. (a) Distinguish between a
(i) parallel and serial register. [4]
(ii) buffer register and jam entry [4]

(b) Show how a 4 - bit register with jam entry is constructed using flip - flop type of your choice. [12]

- END OF EXAMINATION -