NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

APPLIED PHYSICS DEPARTMENT

SPH 2106 – DIGITAL ELECTRONICS

BSc HONOURS PART II: NOVEMBER 2005 *DURATION: 3 HOURS*

ANSWER **ALL** PARTS OF QUESTION **ONE** IN SECTION A AND **ANY THREE** QUESTIONS FROM SECTION B. SECTION A CARRIES 40 MARKS AND SECTION B CARRIES 60 MARKS

SECTION A

1. a) Write the following decimal numbers as binary numbers to 12-bit accuracy
   i. 1562.5 [2]
   ii. 74.8063 [2]

   b) Convert the Gray-coded number 1001101101 to its binary equivalent. [3]

   c) Write the following decimal numbers as BCD coded binary numbers:
   i. 26 [2]
   ii. 527 [2]

   d) Prove the Boolean expression $A \oplus C = A \circ \overline{C} + \overline{A} \circ C$ using truth tables. [3]

   e) Verify $\left(A + \overline{B}\right) \circ \left(\overline{A} + \overline{B} + C\right) = A \circ C + \overline{B}$ using Boolean algebra. [3]

   f) Discuss the difference between sequential and combinational logic. [3]

   g) Give the difference between asynchronous and synchronous counters? [3]

   h) Describe the features of the following memory types:
   i. RAM [2]
   ii. ROM [2]
   iii. PROM [2]
   iv. EPRROM. [2]

   i) Sensors are used to monitor the pressure and the temperature of a chemical solution stored in a vat. The circuitry for each sensor produces a HIGH voltage when a specified maximum value is exceeded. An alarm requiring a LOW voltage input must

be activated when either the pressure or the temperature is excessive. What type of logic gate is required for this application? [3]

j) Draw the block diagrams for parallel in-parallel out and serial in-serial out shift registers. Explain how each of these registers work. [6]

SECTION B

2.

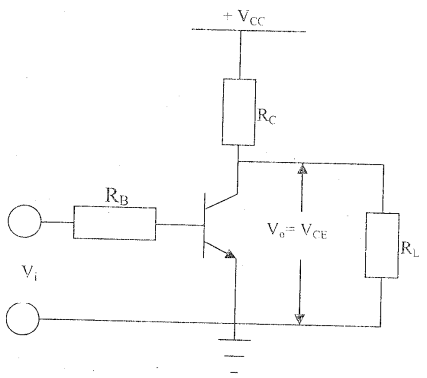

Figure 1: RTL logic NOT gate

The circuit in Figure 1 represents a "loaded" RTL logic NOT gate. If V_{CC} is + 5V, R_C = 1 kΩ, R_B = 50 kΩ,

a) find the value of R_L which would cause the logic level 1 of the output of the gate to fall from + 5V to + 3V. [5]

b) How many identical circuits can the NOT gate be assumed to be driving if the input resistance of a single driven stage is 12 kΩ. [5]

c) What do you understand by the term noise margin? Explain with the aid of a sketch diagram. [5]

d) An ECL circuit has its output voltage levels specified as follows: Nominal logic 0 at -1.58 V, nominal logic 1 at -0.75 V, while for the input the logic 0 voltage may be as low as -1.3 V and the logic 1 voltage maybe as high as -1.0 V. Find the noise margins. [5]

3. a) Draw the circuit diagram of a clocked SR flip-flop using NOR gates and explain circuit action for all combinations of input states. [10]

b) The inputs to a clocked SR flip-flop constructed from NOR gates is as shown in Figure 2. Deduce the Q output from the flip-flop assuming positive-edge triggering and that Q is initially low. [5]
Assume.

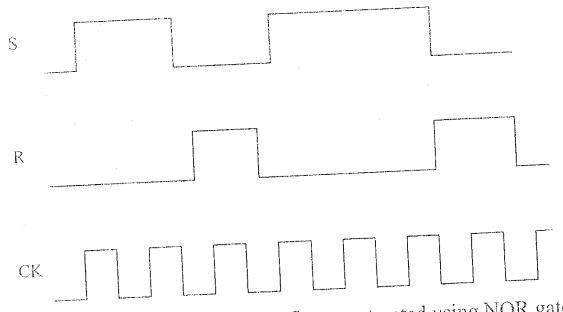

Figure 2: Inputs to a clocked flip-flop constructed using NOR gates

c) What is the advantage in using flip-flops with preset and clear inputs? [2]

d) If the delay time of a single flip-flop in a five-stage counter is 18 ns, what would be the suitable upper frequency limit? [3]

4. a) The Boolean expression for the output Y, from a logic circuit is given by $Y = \overline{A} \cdot B + A \cdot C$.
i. Draw this circuit. [3]
ii. Give the truth table for this circuit. [2]

b) Using a Karnaugh map, write simple sum-of-products expressions for F and $\overline{F}$, where $F = \overline{A} \cdot \overline{D} \cdot B + B \cdot \overline{C}$ and $A \cdot B \cdot C \cdot \overline{D}$ is a "don't care" state. [4]

c) Develop the logic circuit necessary to meet the following requirements:

A lamp in a room is to be operated from two switches, one at the back door and one at the front door. The lamp is to be on if the front switch is on and the back switch is off, or if the front switch is off and the back switch is on. The lamp is to be off if both switches are off or if both switches are on. Let a HIGH output represent the ON condition and a LOW output represent the off condition. [3]

d) State the difference in terms of wiring arrangement, speed and accuracy between

a serial adder and a parallel adder. [8]

5. a) Figure 3 shows a circuit (half adder) for adding two binary digits A and B.

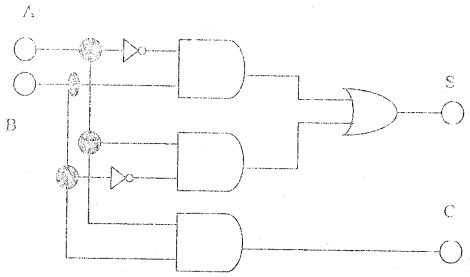

Figure 3: Circuit diagram of a half adder.

i. Express the sum S and carry C as functions of A and B. [4]

ii. Using De Morgan's law or otherwise show how this circuit can also be implemented in NAND gates only. Draw a diagram of such an implementation. [6]

iii. Show how two circuits of this type can be combined with a 2-input OR gate to form a full-adder circuit with inputs A, B and C (carry-in) and outputs S and C_o (carry-out) [3]

b) For a Schmitt trigger circuit with a UTL = 5 V and LTL = 2 V sketch the output waveform. State one application of the Schmitt trigger. [4]

c) Explain the difference between a JK flip-flop and a master-slave RST flip-flop. [3]

6. a) Discuss what is meant by the term "propagation delay" for an asynchronous counter. Why should this effect limit the upper frequency of the input signal? [4]

b) Using a simplified block diagram show how a four-bit shift register may be configured as
i. serial in, parallel-out, ii. parallel-in, serial-out iii. serial-in, serial-out. [6]

c) Give possible applications where each of the registers in (b) above may be used in practice. [6]

d) How do you detect non-monotonic behaviour in a D/A converter? [1]

e) What effect does low gain have on a D/A output? [1]

f) Name two types of output errors in an A/D converter? [2]