# NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

**APPLIED PHYSICS DEPARTMENT**

## DIGITAL ELECTRONICS SPH 2206

## SUPPLEMENTARY EXAMINATION

**BSC HONOURS PART II : JULY 2001** **DURATION: 3 HOURS**

ANSWER **ALL** PARTS OF QUESTIONS 1 IN SECTION A AND ANY **THREE** QUESTIONS FROM SECTION B. SECTION A CARRIES 40 MARKS AND SECTION B CARRIES 60 MARKS.

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### SECTION A

Q1. (a) Determine the resolution of a 12 – bit $D/A$ converter in terms of percentage. [3]

(b) Draw the block diagram of a successive approximation $A/D$ converter. [3]

(c) Show the use of a Schmitt trigger in interfacing systems with transmission lines. [3]

(d) Draw a four – bit parallel adder and determine the sum and carry outputs of each adder for the inputs $A = 1001$ and $B = 1010$ [5]

(e) If the wave forms in fig 1 are applied to an $\bar{S}-\bar{R}$ latch, sketch the resulting $Q$ output waveform in relation to the inputs. Assume $Q$ starts LOW.

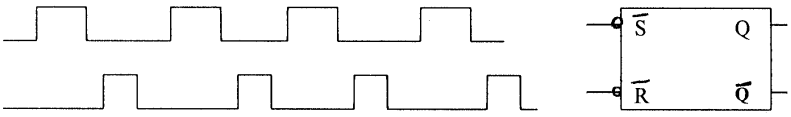


Fig. 1

(f) For the logic circuit in Fig. 2, sketch the output waveform in proper relation to the inputs.

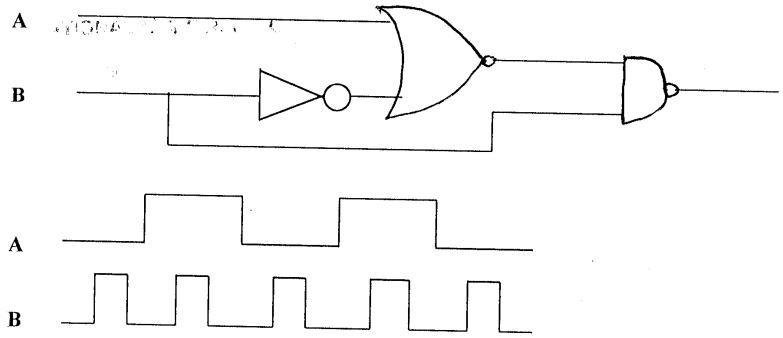


Fig. 2

(g) The simultaneous occurrence of two HIGH level voltages must be detected and indicated by a LOW level output that is used to illuminate an indicator lamp. Sketch the operation. [5]

(h) Simplify the circuit of Fig. 3 as much as possible and verify that the simplified circuit is equivalent to the original by showing that their truth tables are identical.

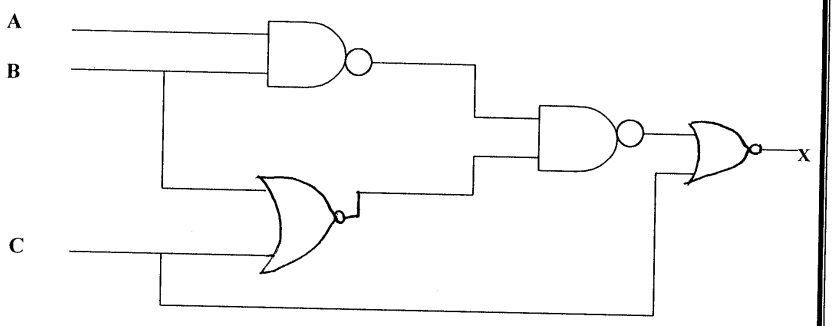


Fig. 3

[5]

(i) For the edge triggered $J-K$ flip-flop with pre-set and clear inputs, determine the '$Q$' output for the inputs shown in the timing diagrams of Fig. 5 $Q$ is initially LOW.

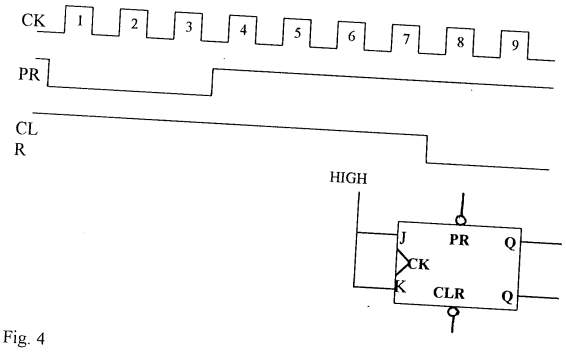


Fig. 4

[6]

## SECTION B

2. (a) A 12-bit D/A converter has an initial accuracy of ¼ LSB and a differential non linearity temperature coefficient of 4.0 ppm /°C. The conveter is to be used in an invironment that goes from + 25°C ≤T ≤ 75°C. Is monotonicity assured. For a 12 - bit converter, 1LSB =244ppm.

[10]

(b) Draw a five-bit register using D-flip-flops. Show the states of the register for the specified data input and clock waveforms shown in Fig. 5. Assume the register is initially cleared (all 0s)

[10]

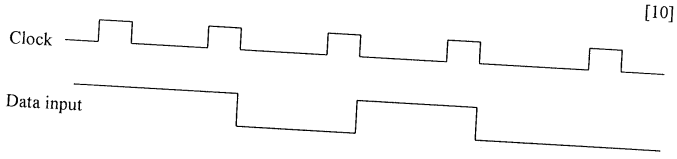


Fig. 5

3. (a) Draw the diagram of a synchronous BCD decade counter. Analyse the operation and draw the timing diagram. [10]

(b) Draw the block diagram of a digital 12 hour clock with six 7 segment readouts. [10]

4. Write brief notes on

(a) parity generators [5]

(b) CMOS inverter [5]

(c) R/2R resistive ladder DAC [5]

(d) Intergrated injection logic ($I^2L$) [5]

5. (a) Draw the diagram of a three stage synchronous binary counter and draw its sequence of states table. [10]

(b) Draw the diagram of a four stage Johnson Counter draw the table of its sequence. [10]

6. (a) Show the J - K flip-flop making transition from RESET to SET state. [10]

(b) A 555 timer is to be used as an unstable multivibrator. Determine the values of $R_1$ and $R_2$ if the output frequency is to be $10kH_z$ with a duty cycle of 50%. The capacitor C is $0,1\ \mu F$. [10]

**END OF PAPER**