NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

APPLIED PHYSICS DEPARTMENT

SPH 2206 DIGITAL ELECTRONICS

BSc HONOURS PART II : MAY 2002 DURATION : 3 HOURS

ANSWER ALL PARTS OF QUESTION 1 SECTION A AND ANY THREE QUESTIONS FROM SECTION B. SECTION A CARRIES 40 MARKS AND SECTION B CARRIES 60 MARKS.

SECTION A

1 (a) Write brief notes on

(i) Small-Scale Integration SSI.

(ii) Medium-Scale Integration MSI

(iii) Logic analyzer. [6]

(b) Discuss the schmitt trigger as an interface circuit [5]

(c) (i) Use Karnaugh Map to find the minimum sum-of-products form for the given expression.

$$X = \bar{A}\left(BC + B\bar{C}\right) + A\left(BC + B\bar{C}\right)$$ [3]

(ii) Simplify, using Boolean algebra:

$$\bar{A}\bar{B}C + \overline{(A + B + \bar{C})} + \bar{A}\bar{B}\bar{C}D$$ [3]

(d) State De Morgan's theorems. Illustrate the use of logic gates to obtain the theorems. [6]

(e) (i) Convert $B2F8_{16}$ to decimal.

(ii) Find $DF_{16} + AC_{16}$.

(iii) Convert from decimal to BCD : 65

(iv) Convert to excess –3 code : 35 [4]

(f) If the input waveforms are applied to the decoding logic, as indicated in fig 1, sketch the output waveform in proper relation to the inputs. [4]

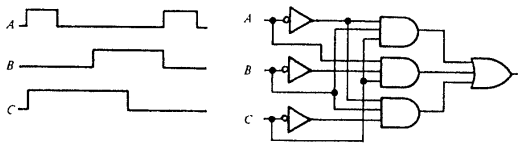
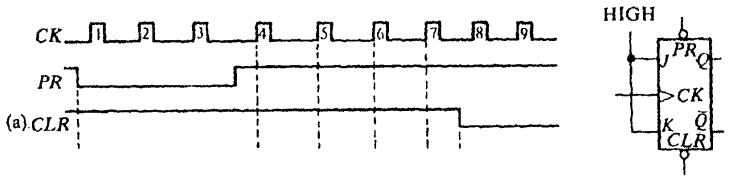


Fig. 1

(g) Using a 555 timer, design an astable multivibrator that will produce a clock signal at a frequency of 10KHz and 50% duty cycle.
Use a 0.1μF capacitor. [5]

(h) For the edge triggered J – K flip – flop with preset and clear inputs, determine the Q output for the inputs shown in the timing diagram of fig 2. Take Q to be initially at a low value.



[4]

Fig. 2

SECTION B

2. (a) Draw the diagram of a BCD decade counter. Analyse its operation and draw the timing diagrams. [10]

(b) Show the master – slave J – K flip-flop, making transition from RESET to SET. [10]

3. (a) Draw the circuit for an R – 2R resistive ladder D/A converter. If R = 10KΩ and V = 10V, determine the analogue voltage given that the digital input is 1001. [10]

(b) Draw a 4 – bit shift register, using J. K. flip-flops. Assume that all the Q outputs are initially clear. The data word to be loaded into the shift register is 0101. Explain how this is achieved. [10]

4. (a) Draw a four-bit parallel adder in the block diagram form. Determine the sum and carry outputs of each adder for the inputs 1011 + 1110. [10]

(b) (i) Apply De-Morgan theorem to the following expression.

$$\overline{A+\bar{B}+C+\bar{D}} + \overline{ABC\bar{D}}$$ [5]

(ii) Convert the following to sum-of-product form and minimise.

$$AB+CD\left(A\bar{B}+CD\right)$$ [5]

5. Write brief notes on

(i) Integrated injection logic (I^2L) [5]
(ii) Parity generaters [5]
(iii) CCD registers [5]
(iv) UART interface [5]

6. (a) Explain the working of a floppy disk used as a memory device [6]

(b) Draw a typical PROM block diagram and write brief notes on the PROM. [8]

(c) Discuss the characteristics of the following: EPROM, UVEPROM, and EEPROM. [6]

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