NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

APPLIED PHYSICS DEPARTMENT

SPH 2206 - DIGITAL ELECTRONICS

BSc HONOURS PART II: JUNE 2004 DURATION: 3 HOURS

ANSWER **ALL** PARTS OF SECTION A AND ANY **THREE** IN SECTION B.
SECTION A CARRIES 40 MARKS AND SECTION B CARRIES 60 MARKS

SECTION A

1. (a) Perform the following operations using 1's and 2s-complement method.
(i) 11100 –1101, (ii) 100001 – 1010, (iii) 10111 – 11111 [6]

(b) Perform the following operation using *BCD* addition.

(i) 00100101 + 00100111
(ii) 01010001 + 01011000
(iii) 11110 + 11011 + 11101 and
(iv) 10111 + 1011 [4]

(d) Write the name *JESUS* in ASCII and EBCDIC code. [8]

(e) Use K-map to simplify the following Boolean expressions:

(i) F(ABC) $= \overline{A}B\overline{C} + \overline{A}BC + 'AB\overline{C} + ABC$

(ii) $F(A,B,C,D) = \sum m(0,1,2,3,4,5,6,7,8,10) + \sum d(9,11,12,14)$

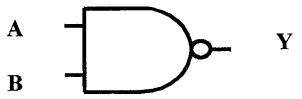
[4]

(f) State and prove De Morgan's theorem. Use the theorem to simplify the following functions:

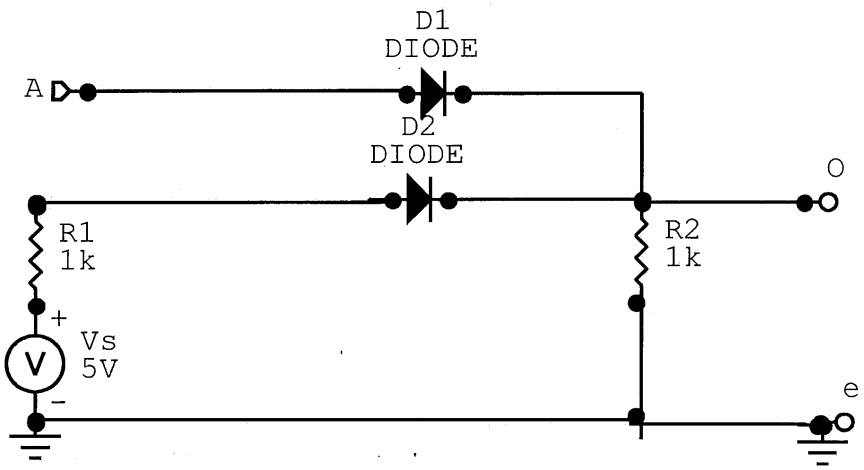
(i) $\overline{(A.B)}.A\overline{(A.B)}B$

(ii) $\overline{A.B} + \overline{\overline{A} + B}$ [4]

(g) How will you realize the following logic using DTL? Give truth table and explain its operation. [6]



(h) Explain the operation of the circuit given below. Calculate the out put voltage at point O. If the logic 1 threshold is 3.8 V, calculate the minimum value of R_2 to obtain logic 1 at the out put. What is the effect of reducing the value of R_1? [8]



SECTION B

2. (a) Show that the "NAND" and "NOR" gates are universal gates. [8]

(b) A circuit is required to monitor an automobile safety belt system. An audio signal should be produced to warn a driver that seat belt is not engaged, when ignition switch is " ON". Alarm should last for specified time and then turn "***off***" automatically. Draw a circuit diagram for this system. Give truth table. [7]

(c) A certain gate draws a current of 2 mA when its output is "HIGH" and 3.5 mA when its output is "LOW". What is the average power dissipation if V_{CC} is 5V and is operated on 50 % duty cycle? [5]

3. (a) What is the difference between half-adder and full adder [4]

(b) Design a " *Half Adder* " using minimum number of "*NOR*" gates only. [8]

(c) Describe the methods of speeding addition. [8]

4. (a) What do you understand by *race around condition* in a flip-flop? How this condition can be avoided? [6]

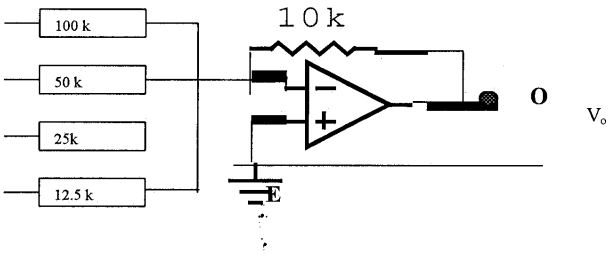
(b) Draw a state and timing diagrams for a BCD decade counter. Explain the operation of a *synchronous* BCD decade counter. [8]

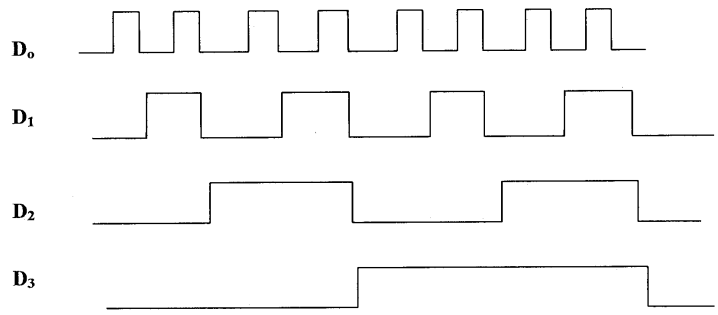
(c) If the ten stage ring counter has the initial stage 1010000000, determine the waveform of the Q outputs. [6]

5. (a) Give the performance characteristics of D/A Converter. [4]

(b) Draw the circuit diagram of a "Four Bit Binary Weighted input D/A converter. Explain its operation. [8]

(c) Determine the output of the D/A converter shown below for the sequence of four bit numbers that are applied to the inputs. D_o is the LSB. [8]





6. (a) Draw a neat diagram of a "*successive approximation*" A/D converter and explain its operation. [10]

(b) Explain the terms:

(i) Resolution,
(ii) Sampling Rate and
(iii) UART [6]

(c) Determine the resolution for each of the following D /A converters.
(i) Four bit,
(ii) six bit and
(iii) 18 bit. [4]

END OF PAPER