NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

APPLIED PHYSICS DEPARTMENT

SPH 2206– DIGITAL ELECTRONICS

BSc HONOURS RADIOGRAPHY: PART II:

APRIL 2014 EXAMINATION **DURATION: 3HOURS**

ANSWER **ALL** PARTS OF QUESTION **ONE** IN SECTION **A** AND ANY **THREE** QUESTIONS FROM SECTION **B**. SECTION **A** CARRIES 40 MARKS AND SECTION **B** CARRIES 60 MARKS.
SHOW ALL YOUR STEPS CLEARLY IN ANY CALCULATION.

SECTION A

1. (a) Briefly explain why D type flip flops are most suitable in the design of shift Registers. [2]

(b) For the pulse shown below in Fig 1, Determine:-

(i) rise time; [2]
(ii) fall time; [2]
(iii) pulse width; [2]
(iv) amplitude of the waveform [2]

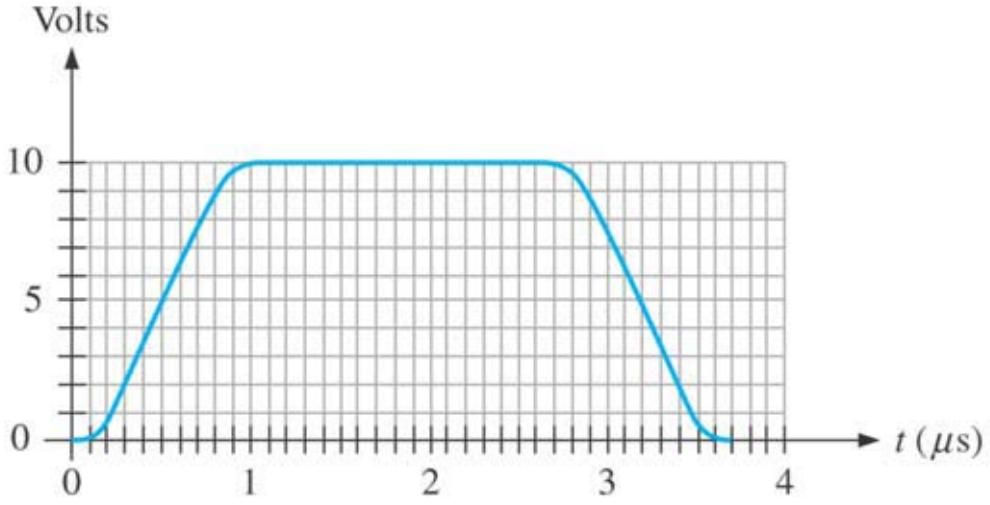

Fig 1: Voltage vs time waveform graph

(c) Convert the following decimal numbers to binary, octal and hexadecimal.

(i) 749.026_{10} [3]

(ii) 657.087_{10} [3]

(d) Convert the following logic gate circuit in Fig 2, into a Boolean expression, writing Boolean sub-expressions for each gate output in the diagram. [6]

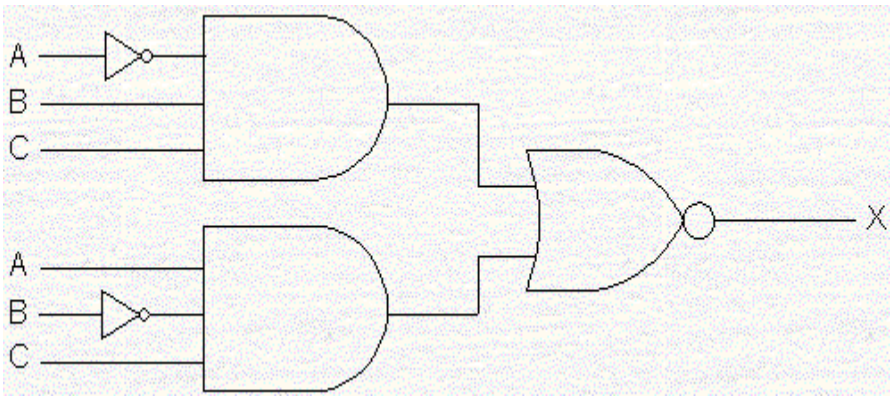

Fig 2: Combinational Logic Circuit

(e) A Radiography engineer hands you a piece of paper with the following Boolean Expression.

$$A\overline{B} + \overline{C}[A + B]$$

Draw a logic gate circuit for this function. [4]

(f) Suppose you needed an inverter gate in a logic circuit, but none were available. You do, however, have spare (unused) NAND gates in one of the integrated circuits.

(i) Show how you would connect a NAND gate to function as an OR gate. [4]

(ii) Use Boolean algebra to show that your solution is valid. [4]

(g) Perform the following subtraction using the 2's compliment method.

(i) $10101_2 - 10111_2$ [2]

(ii) $1111000_2 - 1111111_2$ [2]

(h) Compute a truth tables for the Boolean expression

$$Output = A + \overline{A}B$$ [2]

SECTION B

2. (a) The control logic for an x - ray heating system is to operate as follows: During the daytime, heating is required only if the temperature falls below 68^0C. At night, heating is required only for temperatures below 62^0C. Assume that logic signals D, L, and H are available. D is high during the daytime and low at night. H is high only if the temperature is above 68^0C. L is high only if the temperature is above 62^0C. Design a logic circuit that produces an output signal F that is high only when heating is required. [9]

(b) Define each of the following:

(i) Commutative property [1]
(ii) Associative property [1]
(iii) Distributive property [1]

(c) Implement the following Boolean functions using simple AND, OR and NOT logic gates. (Do not simplify the functions):

(i) $F = AB + ABC + CD$ [2]
(ii) $F = A\,BC + ABC + A\,B$ [2]
(iii) $F = X\,Y\,Z\,(W + YZ) + ZW + X\,Y$ [4]

3. *(a)* Examine the truth table in Fig 3 below.

A	B	C	Output
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Fig 3: Three input Truth Table

(i) Write both SOP and POS Boolean expressions describing the Output [4]

(ii) Which of those Boolean expressions is simpler for this particular truth table? [2]

(ii) Use any technique of your choice to show that the two Boolean expressions are the same. [5]

(b) (i) What is a shift register. [1]

(ii) Explain the operation of the following registers SISO, SIPO, PISO and PIPO. [8]

4. (a) Define each of the following terms as used in digital electronics

(i) Encoder [2]

(ii) Decoder [2]

(iii) Multiplexer [2]

(iv) De-multiplexer [2]

(b) Design a multiplexer with four input data lines and a single output line. [8]

(c) (i) What is meant by the word *resolution* in reference to an ADC or a DAC? [2]

(ii) Why is resolution important to us, and how may it be calculated for any particular circuit knowing the number of binary bits? [2]

5. (a) (i) Design a four-bit binary up counter circuit, using J-K flip-flops. [14]

(ii) Explain what would happen if the upper AND gate's output is to become stuck" in the high state regardless of its input conditions. [2]

(iii) What effect would this kind of failure have on the counter's operation? [2]

(b) Use De – Morgan's theorems to simplify the following expressions:

(i) $F = \overline{\overline{(A+B)}\,\overline{(C+D)}\,\overline{(E+F)}\,\overline{(G+H)}}$ [1]

(ii) $F = \overline{\overline{[\bar{A}+B+C]}\;\overline{[A\bar{B}\bar{C}D]}}$ [1]

6. (a) (i) Compute a truth table for a full adder . [4]

(ii) Obtain the logic expressions for the sum and carry from the truth table. [4]

(iii) Implement the simplified logic circuit. [2]

(b) Draw the circuit diagram of a clocked JK flip-flop using NOR gates and explain circuit action for all combinations of input states. [6]

(c) Simplify the following using K- map

(i) $F = \sum (0, 2, 4, 6, 8, 10, 12, 14)$ [2]

(ii) $F = \Sigma(0,1,2,3,5,7,8,9,10,11)$ [2]

THE END