NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY FACULTY OF APPLIED SCIENCE COMPUTER SCIENCE DEPARTMENT

COMPUTER SCIENCE DEPARTMENT
MAY EXAMINATIONS 2002

SUBJECT: LOGIC DESIGN AND SWITCHING CIRCUITS CODE: SCS 1204

INSTRUCTION TO CANDIDATES

The Question Paper consists of seven (7) questions Answer any five questions.

Time: 3 hours

QUESTION ONE

- a) Devise a truth table for a two input (A and B) logic system whose output is B only if A is zero; otherwise F inverts B. State what type of logic gate would be needed to implement such a system. [4]
- b) A Company is managed by Managing Director Adolfo, a Financial Director Burombo, and two elected members of the board, Chilongo and Dewa. Adolfo needs the support of one other while Burombo needs the support of two others in order to make a decision. Produce a truth table for the decision making strategies, and obtain the logic expressions. [16]

QUESTION TWO

a) Simplify the following Boolean expressions using Boolean theorems.

(i)
$$f = x\overline{y}\,\overline{z} + xy\overline{z} + x\overline{y}z$$

(ii)
$$f = \overline{ABC} + \overline{ABC}$$
 [5]

(iii)
$$ABC + ABE + ABD + AB + ADE + AE$$
 [4]

b) Determine whether the following Boolean identities are valid.

(i)
$$(A+B)(\overline{A}+C) = AC + \overline{A}B$$
 [2]

(ii)
$$\overline{ACD} + \overline{ACD} + ABD + \overline{ABD} = \overline{AD} + B$$
 [5]

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QUESTION THREE

Minimise the following logic functions using the Karnaugh map:

a)
$$\overrightarrow{f} = \overline{A}B + \overline{A}C + B\overline{C} + \overline{B}C + AB + BC$$
 [10]

b)
$$f = \sum m (0,1,2,3,4,5,6,7,8,10 + \sum d(9,11,12,14))$$
 [10]

QUESTION FOUR

Implement the following logic functions using minimum number of NAND gates.

a)
$$f = ABD + ABCD + \overline{A}B\overline{C}D + AB\overline{C}\overline{D} + A\overline{B}D \text{ and don't care } \overline{A}B\overline{D}$$
 [12]

b)
$$f = \sum m(2,3,7,12,13,14,15)$$
 [8]

QUESTION FIVE

- a) Using truth table and reduction methods show clearly how a full adder can be implemented using only three 2 input NAND gates and two Exclusive OR gates. Let A and B be the inputs, C_{in} in the carry from a previous stage, S the sum and C_{out} the carry output.
- b) How could this circuit be adapted for use as a subtractor? [2]

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QUESTION SIX

- a) With the aid of a logic diagram and a truth table, describe the operation of a synchronous Modulo-16 up counter. [14]
- b) Explain with the aid of a logic diagram how an asynchronous Modulo-16 up counter could be converted to a BCD counter.

[6]

QUESTION SEVEN

Show how a 4-bit serial shift register can be constructed using J-K flip-flops.

[8]

b) Show the shift register contents for an input series:

[12]

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END OF QUESTION PAPER

GOOD LUCK!