NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY
FACULTY OF APPLIED SCIENCE
COMPUTER SCIENCE DEPARTMENT
DECEMBER 2002 EXAMINATIONS

SUBJECT: LOGIC DESIGN AND SWITCHING CIRCUITS
CODE: SCS1204

Instructions to candidate:

1. This question paper consists of seven (7) questions.
2. Answer any five questions.

3 HOURS

QUESTION ONE

a) Perform a subtraction with the following binary numbers using 1's complement..

i. 127 – 63 [2]

ii. 93.5 – 42.75 [4]

iii. $84\frac{9}{32} - 48\frac{5}{16}$ [5]

b) Convert the following number from decimal to octal and hexadecimal: 11010111.110 [4]

c) The state of a register is 010110010111.
What is its content if it represents

i. Digits in BCD [2]

ii. Digits in excess –3 code [3]

QUESTION TWO

Design a 5-input logic circuit, 4 inputs (D, C, B, A) of which form the binary representation of a decimal digit. The fifth input is a control input. If the control input is low the output of the circuit should be true only if the decimal input is number 4 or greater. If the control input is high the output should be the reverse of the input bit C. Design the logic circuit using only two input NAND gates. [20]

QUESTION THREE

a) Simplify the following Boolean expressions using Boolean theorems.

i. $\overline{\overline{A}\overline{B}C + \overline{A}B}\,C$ [2]

ii. ABC + ABE + ABD + AB + ADE + AE [2]

b) Minimize the following logic functions using the Karnaugh map:

F = ABD + ABCD + ABCD + $\overline{A}B\overline{C}D$ + $AB\overline{C}\,\overline{D}$ + $A\overline{B}C$ and don't care $\overline{A}B\overline{D}$ [8]

c) Convert the following into sum of products form and minimise using the Karnaugh map.

F = (AB + C) (B + $\overline{C}D$) [8]

QUESTION FOUR

a) Using appropriate truth table and reduction methods, show clearly how a full adder can be implemented using only three 2 input NAND gates and two Exclusive – OR gates. Let A and B be the inputs, C_{in} the carry from a previous stage, S the sum and C_{out} the carry output. [18]

b) How could this circuit be adapted for use as a subtractor? [2]

QUESTION FIVE

a) Starting from the NOR representation of an S-R flip-flop, deduce its characteristic truth table by considering all possible logic levels. [6]

b) Draw the logic diagram of a clocked RS flip-flop with four NAND gates. [4]

c) Derive excitation tables of the following flip-flops.

i. J–K flip-flop [5]

ii. S-R flip-flop [5]

QUESTION SIX

With the aid of the logic diagram and waveforms describe the operation of a modulo-16 down counter. [20]

QUESTION SEVEN

a) Show how a 4-bit shift register can be constructed using J-K flip-flops. [12]

b) Show the shift register contents for an input series. [8]

1	1	1	0	0	0	1	1
t_7	t_6	t_5	t_4	t_3	t_2	t_1	t_0

END OF QUESTION PAPER

GOOD LUCK!