NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY
FACULTY OF APPLIED SCIENCE

COMPUTER SCIENCE DEPARTMENT

AUGUST EXAMINATIONS 2009

SUBJECT: **LOGIC DESIGN AND SWITCHING CIRCUITS**

CODE: **SCS1204**

INSTRUCTIONS TO CANDIDATES

The Question paper contains **six** questions. Answer any **five**.
All questions carry equal marks

3 **hours**

QUESTION ONE

a) Describe the operational characteristics of a clocked D latch. [5]

b) Calculate the number of flip-flops needed to design a counter that can count to denary 128. [3]

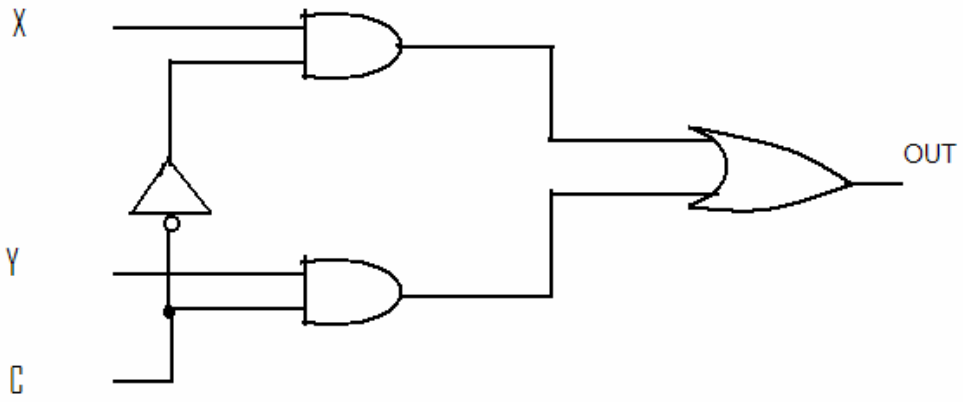
c) Highlight five salient features of TTL and CMOS based integrated circuits [10]

d) a) Reduce the following boolean equation to its simplest form

$$F = (AB + C)(B + \bar{C}D)$$ [2]

QUESTION TWO

The following diagram represents a circuit made out of a combination of four logic gates.



a) (i) Obtain a truth table of the above circuit. [8]

(ii)From your observation on the truth table, what is the effect of the **C** input? [2]

(iii) Name a device that can be implemented by using the above circuit. [1]

b) The table below is a function table of a logical system which is being designed.

A	B	C	Output
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(i) Obtain an expression that represents the sum of products. [4]

(ii) Simplify the resultant sum of products expression and draw a circuit diagram which represents your simplified expression. [5]

QUESTION THREE

a) Give a detailed explanation of the following concepts as used in switching circuits.

(i) Fan out

(ii) Combinational circuit

(iii) Clock

(iv) Race conditions [4]

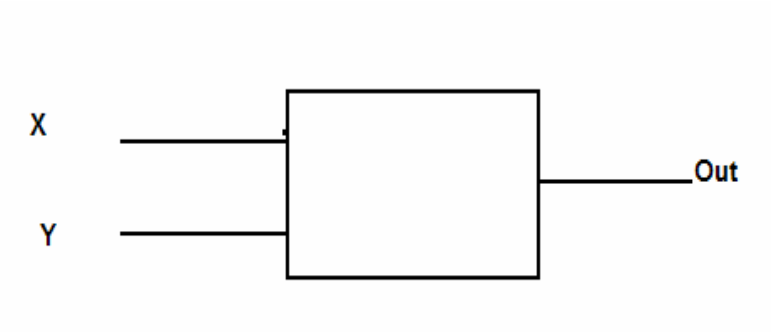
b) With the aid of a diagram, give a detailed explanation of a full adder. [10]

c) Show your understanding of *two's complement* by subtracting denary 11 from 21 in base two. [3]

d) Convert 110111101100_{two} to hexadecimal. [3]

QUESTION FOUR

The illustration below shows a circuit which is under design and the proposed function table for the design.



X	Y	Out
0	0	1
0	1	1
1	0	0
1	1	1

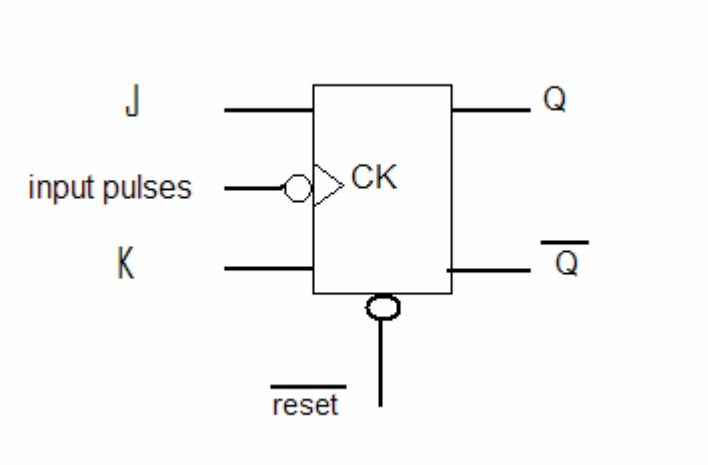
a) With aid of a Karnaugh map, show a combination of logic gates that result from the analysis of the above diagram. [10]

b) State de Morgan's theorems and show the said theorems in a graphic form (Draw diagrams). [4]

c) NOR gates are often referred to as universal logic gates. Explain. [6]

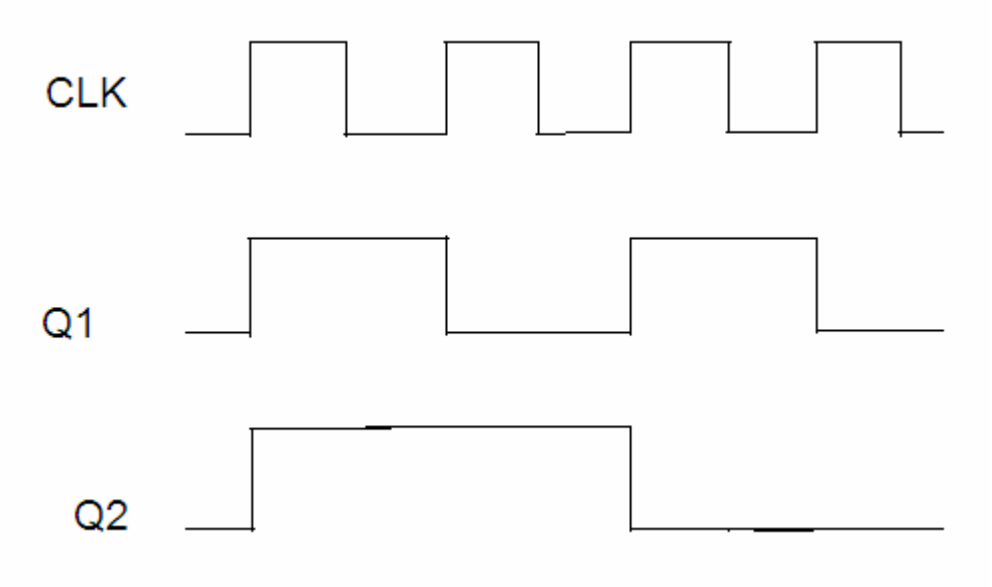
QUESTION FIVE

The diagram below shows a J K flip-flop with a reset capability that can be used as a building block of a counter.



a) (i) What should be the logic level of the J and K inputs in order for the flip-flop to toggle on the clock pulses? [2]

(ii) Clearly showing your outputs, design a ripple counter that will count to 8 giving the following output waveform:



[6]

(iii) Explain how your counter can be adopted to be a countdown counter. [3]

(iv) What will be the effect of placing a logic zero on the reset button? [2]

b) Clearly distinguish between bistable, monostable and astable multivibrators. Which of the multivibrators is also called the *one shot*? [7]

QUESTION SIX

a) Using your knowledge of the NE555 integrated circuit, show how it can be wired to produce a waveform suitable for a clock signal of a ripple counter. [12]

b) Draw a gated SR latch and explain the benefit of gating the latch. [8]

END OF QUESTION PAPER