NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY
FACULTY OF APPLIED SCIENCES

COMPUTER SCIENCE DEPARTMENT

MAY EXAMINATIONS 2011

SUBJECT: LOGIC DESIGN AND SWITCHING CIRCUITS
CODE: SCS 1204

INSTRUCTIONS TO CANDIDATES
This examination paper consists of SEVEN (7) questions, all questions carry equal marks.
Answer any FIVE (5) questions **Time: 3 hours**

QUESTION ONE

a) Describe the following concepts:

i. Combinational circuit [2]

ii. Fan-out [2]

b) Distinguish between:

i. **Overflow** and **carry-over** when these terms are applied to two's compliment arithmetic on n bit words. [2]

ii. Negative and Positive Logic [2]

iii. SIPO and PIPO shift registers [2]

c) With the aid of a diagram, give a detailed explanation of a full adder. [10]

QUESTION TWO

a) Using 8 bit words, represent the number –99 using:

i. The Signed Magnitude representation [2]

ii. The Two's compliment representation [3]

iii. State and explain the properties of two's complement number representation. [5]

b) A logic device has 4 input lines (A, B, C and D) that accept natural numbers in the range 0000_2 to 1111_2 so as to represent decimal numbers 0 to 15. The output (R) of the circuit is true if the input to the circuit represents a prime number and is false otherwise.

i. Design the truth table for this circuit [4]

ii. Design a circuit using AND, OR and NOT gates to carry out this function. [6]

QUESTION THREE

a) i State and explain De Morgan's theorems [3]

ii Using De Morgan's theorems, reduce the following expression to its simplest form:

$$R = (AB + C)(B + \overline{C}D)$$ [3]

iii Using Boolean theorems, simplify the following expression:

$$\overline{\overline{A}\,\overline{B}\,C} + \overline{A\,B}\,C$$ [4]

b) Given the Karnaugh map below, generate a simplified SOP expression and draw the corresponding logic circuit:

$_{AB}\backslash^{CD}$	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	0	1	1
10	1	1	1	1

[7]

c) Compare and contrast the Karnaugh Map and the Truth Table. [3]

QUESTION FOUR

a) Figure 1 shows the timing diagram of a positive edge triggered gated D latch.

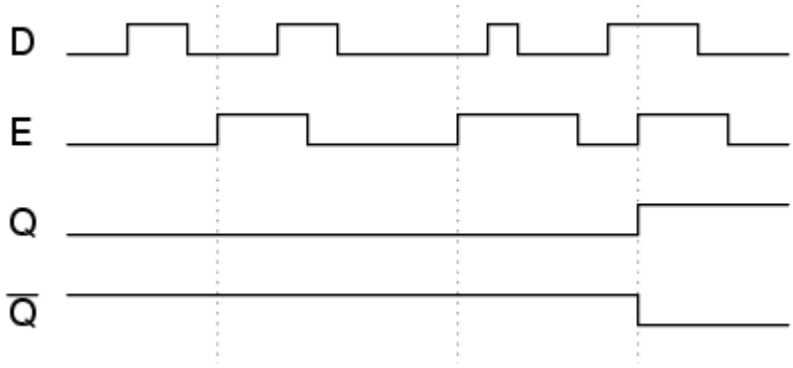

Figure 1

i. Explain the relationship between **D** and **E** [3]

ii. Obtain a function table which involves **D**, **E** and **Q** and $\overline{\mathbf{Q}}$ [4]

iii. Draw the timing diagram of the same latch if it was *negative triggered.* [3]

b) Derive the excitation tables of the following flip-flops:

i. D flip flop [4]

ii. J-K flip- flop [6]

QUESTION FIVE

a) Give brief descriptions and applications of the following devices

i. Multiplexers [4]
ii. Encoders [4]
iii. Code converter [4]
iv. Decoders [4]

b) Explain why NOR gates are often referred to as universal logic gates. [4]

QUESTION SIX

a) Discuss in detail the following logic technologies:

i. TTL [5]
ii. CMOS [5]

b) Draw the TTL internal structure of an XOR gate. [10]

QUESTION SEVEN

An automatic vending machine dispenses a cup of coffee or soup (depending on the customer's choice). Before it delivers coffee or soup, some money (coins) must have been put in, the button for the corresponding choice must have been pressed.

Taking your inputs as coffee button (C), money button (M) and soup button (S), devise a logic gate system for the decision making strategy of the vending machine by coming up with a relevant truth table and drawing a suitable circuit diagram. [20]

END OF QUESTION PAPER