NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY
FACULTY OF APPLIED SCIENCE
COMPUTER SCIENCE DEPARTMENT
DECEMBER EXAMINATIONS 2005

SUBJECT: COMPUTER ARCHITECTURE
CODE: SCS2102

INSTRUCTION TO CANDIDATES

Answer any **FOUR** questions. Paper contains FIVE questions.

Time: 3 hours

QUESTION ONE

a) How many 1024x4 RAM chips are required to make a 4KB of memory? [3]
b) The memory address of the last location of 1KB memory chip is given as FBFFH. Specify the memory map for this chip. [3]
c) Explain the functions of the following signals in an 8085 microprocessor
   i. RESET OUT
   ii. HOLD
   iii. READY [6]

d) Write the machine code for the instruction MOV H, A if the opcode is 01_2, the register code for H is 100_2, and the register code for A is 111_2. [3]

e) The following block of data is stored in memory locations starting from 2055H to 205AH. Write an 8085 assemble language program to transfer the data block to consecutive locations starting from 2080H.

   Data given in hexadecimal: 22, A5, B2, 99 7F, 37. [10]

QUESTION TWO

a) Write comments on each line of the following 8085 assemble language program and explain what the program does [10]

```
Label    opcode    operand      comments
         LXI       B, 208FH     ;
LOOP:    DCX       B
         MOV       A, C         ;
         ORA       B
         JNZ       LOOP         ;
         HLT                    ;
```

b) What are the hardware and software constraints imposed on the design of a Computer System? [10]

c) In the following circuit, Figure 1 what is the address range of selected memory device? [5]

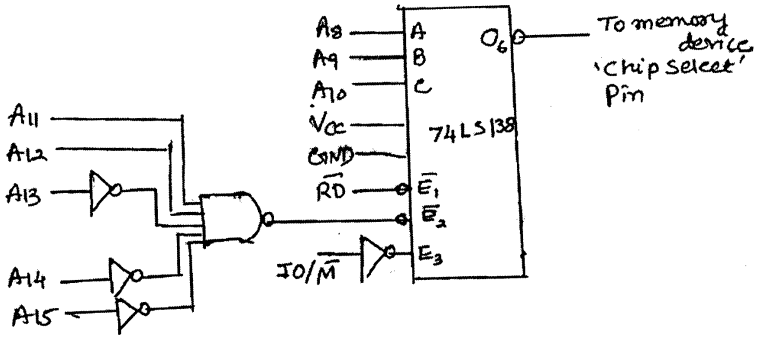

Figure 1

QUESTION THREE

a) With the aid of a timing diagram explain the execution of any 8085 microprocessor instruction [10]

b) Explain the single slope analog to digital conversion technique [8]

c) How many bits will a D/A counter use so that its full-scale output voltage is 5 V and its resolution is at the most 10 mV? [4]

d) If an input and output port can have the same 8–bit address, how does the 8085 differentiate between the ports? [3]

QUESTION FOUR

a) Find out the errors and correct them in following instruction related to 8085 microprocessor:

i. JP 80 H [3]
ii. INX L [3]
iii. MVI B, D [3]
iv. CMA A. [3]

b) What considerations must be made when interfacing the following?

i) DRAM [5]
ii) EEPROM [4]
iii) Input/Output devices [4]

QUESTION FIVE

a) Compare and contrast multiprocessing and parallel processing with reference to computer architecture [10]

b) Describe the way in which a Cache memory operates and explain how it accelerates the running of a program [9]

c) In the context of high performance memory systems, describe the meaning of the following terms:

i) latency
ii) bandwidth
iii) interleaved memory [6]

END OF QUESTION PAPER