NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY
FACULTY OF APPLIED SCIENCE
COMPUTER SCIENCE DEPARTMENT
JANUARY EXAMINATIONS 2013

SUBJECT: **COMPUTER ARCHITECTURE**

CODE: SCS2102

INSTRUCTION TO CANDIDATES

Answer any four questions.
All questions carry equal marks (25)
All programming questions refer to the PIC16F84

Time: 3 hours

QUESTION ONE

Consider a simple Microprocessor system with 256 bytes of memory. Assume this memory chip is made up of one 256x8 RAM chip.

a) Calculate the number of addressable locations in the 256 x 8 RAM chip. [1]
b) Address decoding is needed for a 2K byte memory. This memory is built from 256 x 8 RAM chips.

i. How many 256x8 RAM chips are needed? [1]
ii. What size of decoder is needed to fully address all 2K byte memory? [2]
iii. Assuming that the least significant address bit is A0, which address lines, must be connected to the select lines on the decoder? [1]
iv. Produce a logic diagram illustrating your design for this 2K memory. Also include a memory map in your design. [20]

QUESTION TWO

a) Discuss the interrupt system in the PIC16F84 microcontroller. [8]
b) Outline the ISR of the PIC16F84 microcontroller. [4]
c) Data movement within the CPU can be performed in several different ways. Contrast the following methods in terms of advantages and disadvantages:
i. Dedicated connections
ii. One bus data path
iii. Two bus data path
iv. Three bus data path [8]
d) CISC continues to outpace RISC. Discuss. [5]

QUESTION THREE

a) Show how data transfer from disk to memory is conducted under each of the following I/O services: programmed I/O, interrupt driven I/O and DMA. Show the steps taken in each case. [9]

b) Distinguish between the following :

i. Program counter and stack pointer

ii. Memory mapped I/O and shared I/O

iii. centralized and decentralized bus arbitration [2x3]

c) One of the addressing modes of the PIC16F84 microcontroller is the indirect addressing mode. With the aid of diagram explain how this mode is implemented. [3]

d) Interpret the code given below : [7]

```
movwf h '20',w
subwf h '30' ,w
btfss STATUS, Z
goto LABEL

movlw h '80'
movwf h '40'
goto NEXT

LABEL clrf h '40'

NEXT
```

QUESTION FOUR

a) Why is the memory of a computer system organized in a hierarchy? [2]

b) Describe the basic elements of a memory hierarchy. [4]

c) Explain the operation of Cache Memory. [6]

d) Enumerate and briefly present the 3 types of pipeline hazards. [6]

e) Consider 7 instructions each with an execution time of $T_{ex.}$ They are executed by a 6 stage pipeline. Pipeline overheads are ignored. How long does it take to execute the 7 instructions by the pipelined CPU.(suppose that there are no hazards) [3]

f) Can we conclude that increasing the number of stages always provides increasing performance? Provide arguments. [4]

QUESTION FIVE

K&N Bank wants you to design a system that will be used in the banking hall to alert clients whenever there is a free teller. A 4 bit digital sensor generates a signal to indicate that a teller/s is free or not. If a teller/s is free then an LED comes ON or it is OFF otherwise. Produce a program that would simulate such a system. State any assumptions that you make. [25]

END OF QUESTION PAPER

TABLE 7-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.