NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY **FACULTY OF APPLIED SCIENCE** COMPUTER SCIENCE DEPARTMENT **MAY EXAMINATIONS 2002**

SUBJECT: MICROPROCESSORS AND EMBEDDED SYSTEMS

CODE:

SCS2202

INSTRUCTION TO CANDIDATES

The Question Paper consists of seven (7) questions Answer any five questions.

Time: 3 hours

QUESTION ONE

- Using the block diagram, describe the features of an MC 6800 microprocessor.
- b) Discuss briefly, giving examples, the instruction formats used with MC6800 microprocessor.

QUESTION TWO

- Discuss the various addressing modes used in an MC6800 microprocessor.
- b) Identify the addressing modes used in each of the following MC6800 instructions.
 - (i) **CLRA**
 - LDX%11100001 (ii)
 - (iii) ADDA \$02
 - EORB #\$0A (iv)
- Give the instruction format in hexadecimal for each of the above c) instructions in 4(b) and show the organisation in memory.

QUESTION THREE

Write an assembly language program for an MC 6800 to multiply two numbers less than 16. The two numbers are located in \$70 and \$71 and the result should be stored in \$72.

QUESTION FOUR

- a) With the aid of a diagram, describe the operation of a peripheral interface adapter. [10]
- b) List the steps needed to initialise a port.

[5]

c) Describe the steps taken to clear and set bits in a control register. [5]

QUESTION FIVE

- a) What are the roles of the stack pointer and the program counter? [4]
- b) What are the three phases of executing instructions within the MC6800?
- c) Discuss the actions taken by an MC6800 microprocessor upon receiving an interrupt. [10]

QUESTION SIX

For the MC6800 assembly language program given below:

- a) Find the task performed by the program
- b) Show the organisation of the program in the memory assuming that the program is stored in the memory in locations starting in address 2020#.
- c) Find the memory size required to store the program.

LDX #08H

LDAB #01H

STX 1000H

LOOP INCB

STAB 1001H

E0RB 1000H

BNE LOOP

DEC 1001H

LDAA 1001

DECA

STAA 80H

SWI

QUESTION SEVEN

Write a simple assembly language program that inputs 100 bytes from a port with data register address 1AH and control register address 1BH and stores them in memory locations starting from 2A00H if the data is positive and in memory locations starting from 3A00H if the data is negative.

[20]

END OF QUESTION PAPER

GOOD LUCK!

Appendix A

Instruction Set for 6800 Microprocessor

Accumula	tor and Memory										
Op	Action	Imm	ed	Direct		Exte	Extend		x	Inher	-
code	[1 ₃ 1 1	Hex	#	Hex	#	Hex	#	Hex	#	Hex	#
ADDA	Add	8B	2	9B	3	вв	4	AB	5		
ADDB		СВ	2	DB	3	FB	4	EB	5		
ABA	Add Acmitrs	1								1B .	2
ADCA	Add wth carry	89	2	99	3	В9	4	A9	5		
ADCB		C9	2	D9	3	F9	4	E9	5		
ANDA	And	84	2	94	3	В4	4	A4	5		
ANDB		C4	2	D4	3	F4	4	E4	5		
BITA	Bit Test	85	2	95	3	B5	4	A5	5	-	
вітв		C5	2	D5	3	F5	4	E5	5		
CLR	Clear					7F	6	6F	7		
CLRA						1				4F	2
CLRB								ĺ		5F	2
CMPA	Compare	81	2	91	3	В1	4	A1	5		
СМРВ		C1	2	D1	3	F1	4	E1	5		
CBA	Compare Acmitrs					ļ				11	2
сом	Complement, 1's					73	6	63	7		
COMA		1								43	2
сомв										53	2
NEG	Complement, 2's					70		60			
NEGA	(Negate)									40	2
NEGB				1						50	2
DAA	Decimal Adjust,A	:				ŀ				19	2
DEC	Decrement					7A	6	6A	7		
DECA										4A	2
DECB										5A	2
EORA	Exclusive OR	88	2	98	3	В8	4	A8	5		
EORB		C8	2	D8	3	F8	4	E8	5		
INC	Increment					7C	6	6C	7		
INCA										4C	2
INCB										5C	2
LDAA	Load Acmitr	86	2	96	3	В6	4	A6	5		

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Index Register and Stack

Ор.	Action	Immed		Direct		Extend		Index		Inher	
code		Hex	Hex # Hex # He		Hex	#	Hex	#	Hex	#	
CPX 10	Compare Index Reg	8C	3	9C	4	вс	5	AC	6		
DEX	, Decrement Ind Reg									09	4
DES	Decrement SP									34	4
INX	Increment SP					٠.				08	4
LDX	Load Index Reg	CE	3	DE	4	FE	5	EE	6		
LDS	Load Stack Pntr	8E	3	9E	4	BE	5	ΑE	6		
STX	Store Index Reg			DF	5	FF	6	EF	7		
STS	Store Stack Pntr			9F	5	BF	6	AF	7		
TXS	Indx Reg to SP									35	4
TSX	SP to Ind Reg									30	4
										1	

Jump and Branch

	Jump and	Branch									
	Ор	Action	Rela	tive	Exter	nd	Index			Inhe	
١	code		Hex	#	Hex	#	Hex	#		Hex	#
	BRA	Branch always								20	4
	всс	Branch if carry clear				l				24	4
Ì	BCS	Branch if carry set								25	4
ļ	BEQ	Branch if = Zero								27	4
	BGE	Branch if >= Zero				- 1		l		2C	4
	BGT	Branch if > Zero								2E	4
	вні	Branch if Higher								22	4 ′
	BLE	Branch if <= Zero								2F	4
	BLS	If Lower or same				ĺ				23	4
	BLT	Branch if < Zero				İ				2D	4
	вмі	Branch if Minus				l				2B	4
1	BNE	Branch if not = Zero								26	4
-	BVC	If Overflow Clear								28	4
	BVS	If Overflow Set								29	4
١	BPL	Branch if Plus								2A	4
	BSR	Br to Subroutine								8D	8
1	JMP	Jump			7E	3	6E	4			
	JSR	Jump to subroutine			BD	3	AD	4			,
- 1					1		l		ļ		

									IV	iicropr	oces	sor A	pplic
. Op		Action		Imi	ned	Dir	ect	Exte		Τ.			
LDA				He	4	1	<u>«</u> #	Hex		Inde		Inhe	er
ORA		ANOTHE !	1. 5	Ç6	, 2 !	D6	3	F6	4	Hex	#	Hex	(#
ORA		Or, inclusive		8A	2	9A	3	BA		E6	6		
PSH	- 1	190		CA	2	DA	3	FA	4 4	AA	5		
PSH	- 1	Push Data	1				1	' ^	4	EA	5		
PULA	- 1		- 1						- 1			36	4
PULE	1	Pull Data	- 1								- 1	37	4
ROL	,		- 1		- 1		- 1		- 1		- 1	32	4
ROLA	. 1	Rotate Left	- 1		- 1		- 1.	79 6			- 1	33	4
ROLB	- 1						- 1		10	9 7	- 1		
ROR		_									- 1		2
RORA		Rotate Right					7	6 6			5	9 :	2
RORB							- 1	0 0	66	5 7	-		
ASL			- 1		- 1		- 1				41	-	2
ASLA		Shift Left,					78	3 6	00	_	56	3 2	:
ASLB	- 1	Arithmetic			- 1		- '`	, 0	68	7			1
ASR		0.									48	_	
ASRA		Shift right,			-		77	6	67	_	58	2	
ASRB	1 '	Arithmetic			- 1		'	Ū	67	7			
LSR	1.		-				-				47	2	
LSRA	- 1	Shift Right,	1		1		74	6	64	_	57	2	
LSRB		ogic			1		1.,	U	164	7			1
STAA	1_		1		1		1		1		44	2	
STAB	S	tore Acmitr.			97	4	B7	5	A7	_	54	2	
SUBA					D7	4	F7	5	E7	6			
SUBB	Si	btract	80	2	90	3	Во	4	A0	6			
SBA	1		Co	2	DO	3	FO	4	E0	5			
SBCA								1	CU	5			
SBCB	Su	btract with carry	82	2	92	3	B2	4	A2	ı	10	2	
TAB	_		C2	2	D2	3	F2	- 1		5			
TBA	Tra	nsfer Acmitrs	1				-	٦ '	=2	5			
1 1								- 1		- 1		2	
TST	Tes	t, Zero or Minus					7D	6 6	ъ.	- 1	17	2	
TSTA TSTB							, 5	ء ا	D :	7			
1318										- 1		2	
		J								5	D .	2	

Ор	Action	Relative		Extend		Index		Inher	
code		Hex	#	Hex	#	Hex #		Hex	#
NOP	No Operation	2.3	₹.,					01	2
RTI	Return From Int							3B	10
RTS	Return From Subr	'				1		39	5
SWI	Software Interrupt							3F	12
WAI	Wait for Interrupt							3E	9
							Ì		
								<u> </u>	

Conditions Code Register

Ops	Action	Inhe	<u> </u>	٦	
		Hex	Hex#		
CLC	Clear Carry	0C_	_2_	-	
CLI	Clear interrupt	0E	2	١	
CLV	Clear Overflow	0A	2		
SEC	Set Carry	0D	2		
SEI	Set Interrupt Mask	0F	2		
SEC	Set Overflow	0B	2	١	
TAP	Acmitr to A CCR	06	2		
TPA	CCR to Acmitr A	07	2		
1					

*LIBRARY PTS