NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY
FACULTY OF APPLIED SCIENCE
COMPUTER SCIENCE DEPARTMENT
MAY EXAMINATIONS 2002

SUBJECT: ADVANCED ARCHITECTURE AND OPERATING SYSTEMS
CODE: SCS4201

INSTRUCTION TO CANDIDATES
The Question Paper consists of seven (7) questions
Answer any five questions.

Time: 3 hours

QUESTION ONE

A RISC machine incorporates a register file within its architecture. The file is organised as three overlapping windows W_0, W_1, and W_2, each comprising 9 registers. Three registers must be made available for passing parameters, from a calling function to a called function.

a) By means of a diagram, show how this register file must be configured as a conceptually circular scheme. Explain the role of the three regions in each window. [6]

b) A sequence of function calls (denoted by 'c') and function returns (denoted by 'r') now occurs as follows:

c, c, r, c, c, r, c, r, r, r

Write down in tabular form the contents of the Current Window Pointer (CWP) following each call and return. Indicate where window overflow and underflow occurs. Assume execution starts with CWP = 0. [10]

c) Why does overflow and underflow occur, and how must these events be handled? [4]

QUESTION TWO

a) (i) Briefly describe structural hazards, data hazards and control hazards in a pipelined computer. [6]

(ii) What is meant by 'load delay slots' and 'branch delay slots'? [2]

b) Use the section of mock code below to illustrate how this code could be re-organized by a Re-organising Compiler to remove the inherent data and control hazards. You are being asked to

(i) identify the hazards and delay slots and
(ii) Explain how the hazards can be removed

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LOAD R1, A  (Load contents of address A into R1)
LOAD R2, B
MULT R1, R2, R3 (Multiply R1 by R2 and put result in R3)
ADD R3, R2,R3 (R3: =R2 + R3)
LOAD R4, C
SUB R3, R4, R2 (Subtract R3 from R4 and put result in R2)
BRNEG Q (Branch if negative to instruction at address Q)
SUB R4, R3, R1
BRNEG S
STORE R1, A (Store value of R1 into address A)
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[12]

QUESTION THREE

a) Define the principle of locality. [2]

b) What are the economic and performance implications of using cache memory between the CPU and main memory in a computer system? [4]

c) define the Hit Ratio and explain how it depends on the locality of the programs being executed. [3]

d) A memory cache uses a seven bit TAG to identify block frames in a direct-mapping system. If blocks are eight WORDS in size, and the BLOCK part of the address is seven bits, calculate the sizes of the main memory and cache in words. [6]

e) In a certain computer, the access time to the main memory is eight clock cycles, while that to the cache is tow cycles. If the average cache hit ratio is 75%, calculate the average time (in cycles) for the CPU to access a byte. [5]

QUESTION FOUR

a) Draw a block diagram of the basic architecture of a Von Neumann machine. [5]

b) What are the advantages and disadvantages of a microcoded instruction decoder, versus a hard-wired one? [5]

c) Give in details the distinction between RISC and CISC architecture. [10]

QUESTION FIVE

a) Compare and contrast parallel processing and networking. [4]

b) Distinguish among multiprocessor systems, local area networks, wide area networks and interconnected WAN in terms of the following:

node spacing, communication, services and problems. [16]

QUESTION SIX

a) With the aid of a diagram, describe the basic architecture and operation of an IMMOS Transputer. [14]

b) Discuss the most common applications of the Transputer. [6]

QUESTION SEVEN

a) Describe the operation of the following types of computer architecture;

(i) Single Instruction Single Data (SISD)
(ii) Multiple Instructions Multiple Data (MIMD) [8]

b) Draw a diagram of an array processor and describe its operation. [12]

END OF QUESTION PAPER

GOOD LUCK!