NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

FACULTY OF APPLIED SCIENCE

DEPARTMENT OF COMPUTER SCIENCE

COMPUTER ARCHITECTURE AND ORGANISATION

SCS1216

Examination Paper

March Intake Part I Second Semester Phase II 2024

This examination paper consists of 4 pages

Time Allowed: **3 hours**

Total Marks: **100**

Examiner: **Tsitsi Zengeya**
External Examiner: **Dr Cross Gombiro**

INSTRUCTIONS

1. Answer any four (4) questions
2. Each question carries 25 marks

MARK ALLOCATION

QUESTION	MARKS
1.	**25**
2.	**25**
3.	**25**
4.	**25**
5.	**25**
TOTAL	**100**

QUESTION ONE

a) Explain the difference between the following terms and concepts.

i. Computer Architecture and Computer Organization [2]
ii. Single interrupt and multiple interrupts [2]
iii. single-core computer and a multi-core computer [2]
iv. OR and XOR logic operators [2]
v. Cache memory and Registers [2]
vi. Destination and source operand [2]

b) Given the following Boolean functions do the following:

$$A\overline{B}C + \overline{A}BC + AB\overline{C} + \overline{A}\,\overline{B}C + A\overline{B}\,\overline{C} \quad [6]$$

i. Represent the corresponding combinatory circuit with logic gates [6]
ii. Perform the algebraic and Karnaugh Map simplifications. [7]

QUESTION TWO

a) Explain the function of cache memories in multi-core computers [5]

d) Implement the following Boolean functions with logic gates

i) $$\overline{\left(\overline{(A\overline{B} + C)D}\right) \oplus ((\overline{CD} + B) + A))} \quad [5]$$

ii) $$\overline{\overline{((A + \overline{B})(AB)}} + \overline{(A + B)\,\overline{(\overline{A}B)}} \quad [5]$$

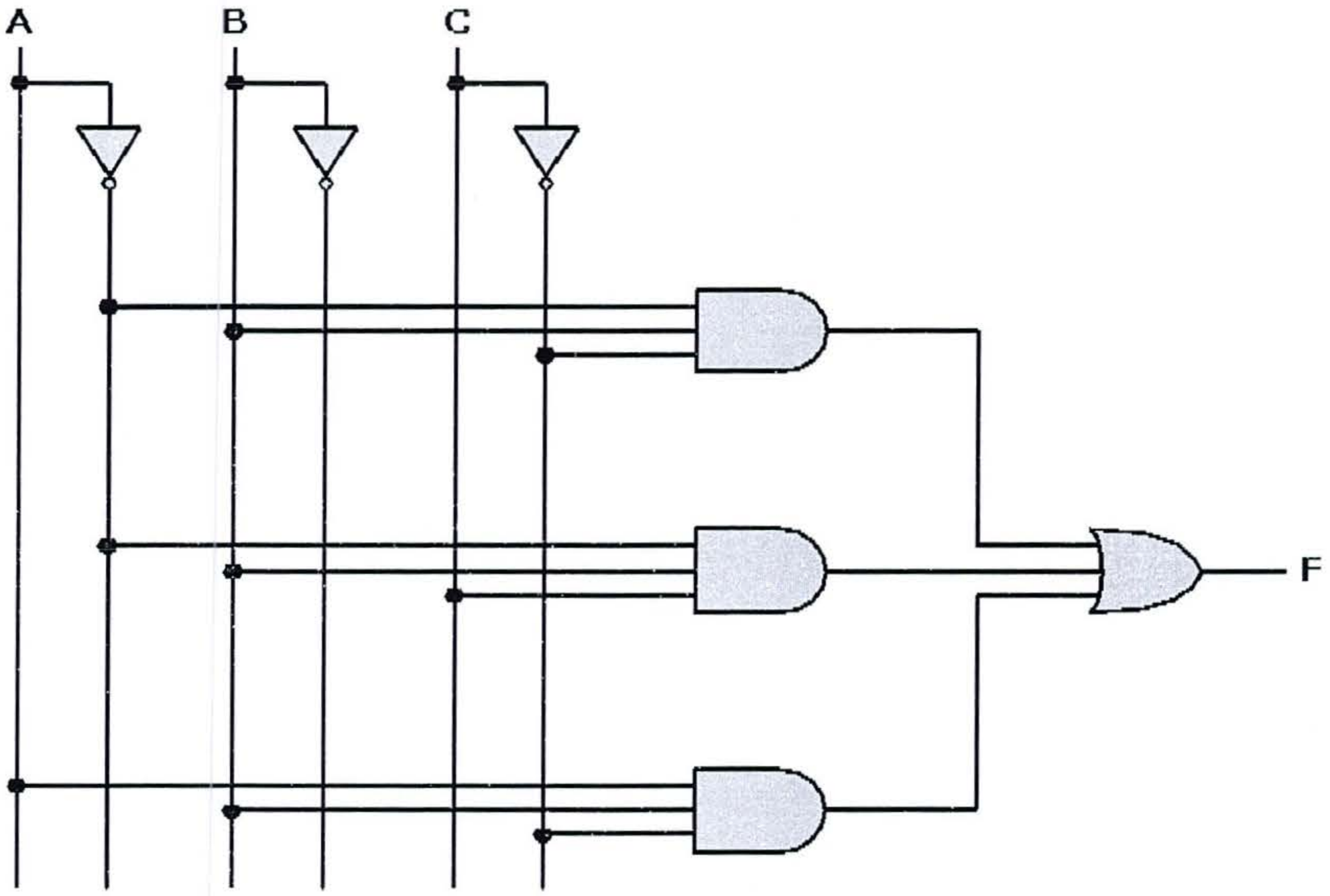
c) State and explain the key characteristics of a computer family. [10]

QUESTION THREE

a) Briefly discuss the PCIe protocol layers. [5]

b) Explain the possible states that define an instruction execution process. [10]

c) Derive the Boolean function and draw a truth table implemented by the following combinatory circuit. [10]



QUESTION FOUR

a) Explain the functions of the following registers during instruction execution.

i. PC [1]
ii. IR [1]
iii. AC [1]
iv. MAR [1]
v. I/O AR [1]
vi. MBR [1]

b) Convert the following numbers to their hexadecimal equivalent.

i. 431.25_{10} [3]
ii. 110101.011001_2 [3]

c) Discuss two approaches that can be used to deal with multiple interrupts. [5]

d) Briefly discuss the main structural components of a processor [8]

QUESTION FIVE

a) Solve the expression $\mathbf{304_{10} - 76_{10}}$ using two's complement. [4]

b) For the following Boolean functions

$$(A\overline{B}\,(C + BD) + \overline{A}\,\overline{B})C$$

i. Represent the corresponding combinatorial circuit with logic gates. [6]

ii. Perform the algebraic and Karnaugh Map simplifications [7]

c) Explain the types of instructions in the 8086 architectures. Illustrate each type of instruction with two examples [8]

END