NATIONAL UNIVERSITY OF SCIENCE AND TECHNOLOGY

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRONIC ENGINEERING

Computer Architecture and Operating Systems

EEE 3231

Final Examination Paper

MARCH 2025

This examination paper consists of 5 pages

Time Allowed: **3 hours**

Total Marks: **100**

Special Requirements: None

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INSTRUCTIONS

1. Answer **ANY FOUR QUESTIONS.**
2. Each question carries 25 marks.

MARK ALLOCATION

QUESTION	MARKS
1	**25**
2	**25**
3	**25**
4	**25**
5	**25**
6	**25**
TOTAL	**100**

QUESTION 1

a) Explain the following types of ROM:

i) PROM

ii) EPROM

iii) EEPROM [3]

b) Describe the role of device controllers. [2]

c) Define a device driver and differentiate between a device driver and device controller. [3]

d) Explain why the SCAN algorithm is also referred to as the Elevator algorithm. [1]

e) Consider an imaginary disk with 71 cylinders. The current head position is at 21. Requests for data on disk then arrive in the following order: 4,35,17,30, 7, and 25. What is the seek time in terms of cylinders using each of the following algorithms?

i) First Come First Serve

ii) Shortest Seek Time First

iii) CSCAN

iv) CLOOK [12]

f) Based on the calculations made in (e) above, give a comparative analysis of the algorithms. [4]

QUESTION 2

a) Define deadlock in operating system and explain one way to handle deadlocks. [3]

b) Name and explain the four necessary conditions for deadlock to occur in operating system. Illustrate with an example from the Dining Philosophers problem. [12]

c) Define the Bankers algorithm and describe the steps that the algorithm uses to grant request. [10]

QUESTION 3

a) Describe and explain the need for memory management is operating systems. [5]

b) Describe and explain the difference between physical and virtual memory in a computer system. [4]

d) In an operating system, page replacement refers to a scenario in which a page from the main memory should be replaced by a page from secondary memory. Page replacement occurs due to page faults.

Describe and explain with the aid of diagrams the five algorithms used in page replacement below.

i) First In First Out (FIFO)

ii) Optimal page replacement

iii) Last In First Out (LIFO)

iv) Random page replacement [16]

QUESTION 4

a) Explain the purpose of the following Von Neumann architecture components in relation to the fetch-decode-execute cycle:

i) Buses [6]

ii) Arithmetic and logic unit [2]

iii) Control Unit [2]

iv) Memory address register [2]

b) What is pipelining? [2]

c) Three instructions are fetched, decoded, and executed using a pipelined approach. The processing times of each instruction are tabulated below, in terms of clock cycles:

Instruction	**Stage**	**Clock cycles**
IA	Fetch	2
	Decode	4
	Execute	3
IB	Fetch	5
	Decode	1
	execute	3
IC	Fetch	4
	Decode	2
	Execute	5

i) How many clock cycles does it take to process the three instructions using a pipelined machine? [3]

ii) Make a comparison with the execution of the same set of instructions using a Von Neumann machine. In your comparison, clearly show how you arrived at the conclusion. [3]

d) Harvard machines are said to be better machines than Von Neumann machine. Is this true or false? Support your answer. [5]

QUESTION 5

a) Process scheduling algorithms are either pre-emptive or non-preemptive. Explain the difference between these two categories of process scheduling algorithms. Give one example algorithm for each category. [4]

b) Describe, using an illustrative example, the following scheduling algorithms. In description, clearing indicate how one can arrive at average waiting time and average turnaround time.

i) Shortest Job First

ii) Priority Scheduling

iii) First Come First Serve [16]

c) Based on examples in (b) compare the performance of these algorithms. [5]

QUESTION 6

a) Distinguish between a PAN, MAN and WAN. [3]

b) Describe the following LAN topologies. In your description, provide one advantage and one disadvantage of the topology.

i) Bus topology

ii) Star topology

iii) Hybrid topology `[15]

c) State and briefly explain the different layers of the OSI network model. [7]

END OF EXAMINATION PAPER